Code : 041504

B.Tech 5th Semester Exam., 2018

ANALOG ELECTRONICS

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

*(ii) There are **NINE** questions in this paper.*

*(iii) Attempt **FIVE** questions in all.*

(iv) Question No. 1 is compulsory.

1. Choose the correct answer (any *seven*) : 2×7=14

(a) For the BJT circuit (Fig. 1) shown below, assume that the β of the transistor is very large and $V_{BE} = 0.7$ V :

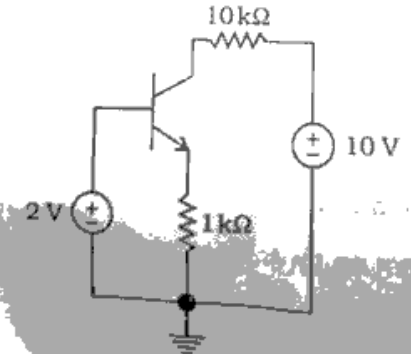

Fig. 1

(e) The small-signal gain of the amplifier V_C / V_S is

(i) –10

(ii) –5·3

(iii) 5·3

(iv) 10

(f) The value of C required for sinusoidal oscillations of frequency 1 kHz in the circuit shown in Fig. 4 is

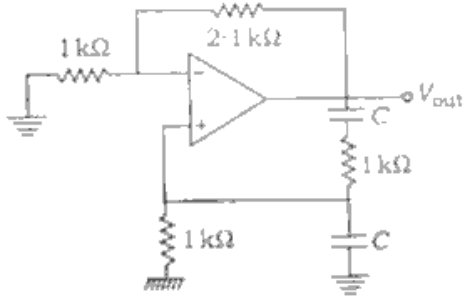

Fig. 4

(i) $\frac{1}{2\pi}\mu F$

(ii) $2\pi\ \mu F$

(iii) $\frac{1}{2\pi\sqrt{6}}\mu F$

(iv) $2\pi\sqrt{6}\ \mu F$

(Continued)

The mode of operation of the BJT is

(i) cut-off

(ii) saturation

(iii) normal active

(iv) reverse active

(b) Assuming $V_{CE,\,Sat} = 0{\cdot}2\ V$ and $\beta = 50$, the minimum base current (I_B) required to drive the transistor in the given figure (Fig. 2) to saturation is

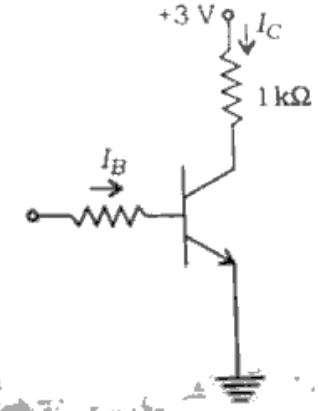

Fig. 2

(i) 56 μA

(ii) 140 μA

(iii) 60 mA

(iv) 3 mA

(i) In Fig. 4, transconductance in millisiemens (mS) and voltage gain of the amplifier are, respectively

(i) 1·875 mS and 3·41

(ii) 1·875 mS and −3·41

(iii) 3·3 mS and −6

(iv) 3·3 mS and 6

(j) The cascade amplifier is a multistage configuration of

(i) CC-CB

(ii) CE-CB

(iii) CB-CC

(iv) CE-CC

2. *(a)* Explain class B transformer-coupled amplifier with circuit diagram.

(b) A transformer-coupled class A amplifier suppli...

(c)

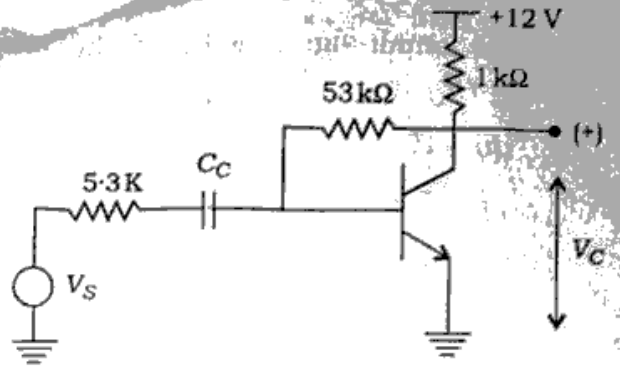

Fig. 3

In the transistor amplifier circuit shown in Fig. 3 the transistor has the following parameters :

$\beta_{DC} = 60$, $V_{BE} = 0 \cdot 7$ V, $h_{ie} = \alpha$, $h_{fe} = \alpha$

The capacitance C_C can be assumed to be infinite. Under DC conditions, the collector to emitter voltage drop is

(i) 4·8 V *(ii)* 5·3 V

(iii) 6 V *(iv)* 6·6 V

(d) In Fig. 3, if β_{DC} is increased by 10%, then collector to emitter voltage drop

(i) increases by less than or equal to 10%

(ii) decreases by less than or equal to 10%

(iii) increases by more than 10%

(iv) decreases by more than 10%

(g)

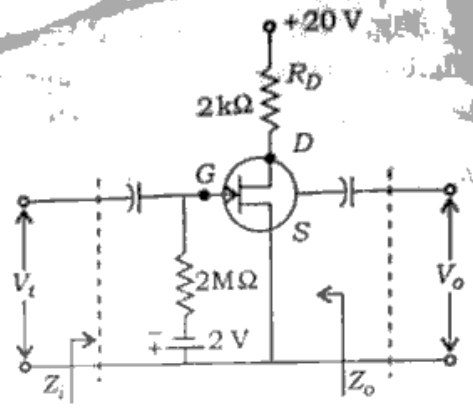

Fig. 5

Given $r_d = 20$ kΩ, $I_{DSS} = 10$ mA, $V_p = -8$V, Z_i and Z_o of the circuit are, respectively

(i) 2 MΩ and 2 kΩ

(ii) 2 MΩ and $\frac{20}{11}$ kΩ

(iii) infinity and 2 kΩ

(iv) infinity and $\frac{20}{11}$ kΩ

(h) I_D and V_{DS} in Fig. 4 under DC conditions are, respectively

(i) 5·625 mA and 8·75 V

(ii) 7·5 mA and 5 V

(iii) 4·5 mA and 11 V

(iv) 6·250 mA and 7·5 V

circuit diagram.

(b) In a BJT-based R-C phase-shift oscillator, $R = 200\ k\Omega$, $C = 200\ PF$. Find the frequency of the BJT-based oscillator. 7+7=14

4.

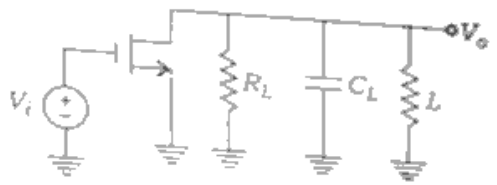

Fig. 6

It is required to design a tuned amplifier of the type shown in Fig. 6, having $f_0 = 1$ MHz, 3 dB bandwidth = 10 kHz, centre frequency gain = −10 V/V. The FET available has at the bias point $g_m = 5$ mA/V and $r_0 = 10\ k\Omega$. The output capacitance is negligibly small. Determine R_L, C_L and L. 14

5. Draw the small-signal equivalent circuit of common-emitter amplifier and derive the expression for *(a)* current gain, *(b)* input resistance and *(c)* voltage gain. 14

6. Draw the hybrid-π model for a transistor in the CE configuration and discuss about each parameter. 14

7. Explain the effect of an emitter bypass capacitor on low frequency response of a BJT-based basic amplifier. 14

8. Explain the operation of common-base configuration of BJT and draw the input-output characteristics. Also explain the early effect. 14

9. Write short notes on the following : 7+7=14

(a) Ideal voltage amplifier

(b) Ideal transconductance amplifier

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